Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 2 and 4 - 11 are presently pending in the application. Claims 1 and 5 have been amended. Claim 3 was previously canceled. New claims 8 - 11 have been added.

In item 3 of the above-identified Office Action, claims 1 - 2 and 4 - 7 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U. S. Patent No. 5,305,261 to Furutani et al ("**FURUTANI**").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

As stated on page 4 of the instant application, lines 4 - 17, in bidirectional input/output circuits (i.e., wherein the input terminal is connected to the output terminal and to an output line) is concomitantly driven when driving an output signal, use more current than is necessary to supply the system. More particularly, page 4 of the instant application, lines 4 - 17, states:

> Provision may be made for the input circuit to be contained in a bidirectional input/output circuit. **It is frequently the case with bidirectional input/output circuits that the input circuit, which is connected to**

> **the respective external terminal in parallel with the output driver, is concomitantly driven when driving an output signal with the aid of the output driver.** The input circuit then receives the signal which has been driven onto the output line and makes it available at the output node of the input circuit, which node, in this case, **is decoupled from the circuits in the integrated circuit, with the result that the signal does not trigger a function. Increased current drawing is thus also affected in a bidirectional input/output circuit when signals from the integrated circuit are to be driven onto an external line.** [emphasis added by Applicants]

As such, known bidirectional input/output circuits waste current by providing a signal that does not trigger a function.

Applicants' invention of claims 1 - 7 addresses the shortcomings of the prior art by reducing the unnecessary current drawn by the bidirectional input/output circuit.

More particularly, claim 1 has been amended to recite an input circuit that is part of a bidirectional input/output circuit, wherein, among other limitations,:

> said input circuit being deactivated based on said activation signal **such that the deactivated input circuit does not draw any quiescent or switching current as a result of the detection of received signals.** [emphasis added by Applicants]

Applicants' independent claims 5 and 7 contain similar limitations, among others. Applicants' amended claims are

supported by the specification of the instant application, page 3, line 10 - page 4, line 2, which states:

> According to the invention, an integrated circuit has thus been provided with an input circuit **which can be deactivated, with the result that the input circuit does not draw any quiescent current and, respectively, does not draw any switching current as a result of the detection of the applied signal**, which currents load the power supply, even though the input signal is not required in the integrated circuit in question.
>
> Provision may preferably be made for the input circuit to be connected in such a manner that **the input circuit may be switched on or off with the aid of the activation signal**. That is to say, **the input circuit is connected to the power supply or disconnected therefrom depending on the activation signal. This makes it possible, in a very effective manner, to deactivate the input circuit and thus ensure that no current flows through the input circuit when the input signal changes state.** [emphasis added by Applicants]

As such, as stated on page 2 of the instant application, lines 24 - 26, the present invention overcomes the disadvantages of the prior art devices, reducing the current consumption of the integrated circuit.

The **FURUTANI** reference mainly discloses a semiconductor memory device **not including** a **bidirectional** input/output circuit. Rather, as described in col. 12 of **FURUTANI**, lines 61 - 68:

> Input/output circuit 6 produces an external data Dout from the data read onto internal data transmitting lines IO and /IO in a data writing operation. In the data writing operation, it responds to a write instructing signal /WDE to produce an internal write data from an external write data Din. The internal

> write data thus produced is transmitted to internal data transmitting lines IO and /IO.

Thus, in the main, **FURUTANI** does not describe a bidirectional input/output circuit (i.e., wherein the input terminal is connected to the output terminal and to an output line) and does not recognize the problems with such a bidirectional circuit. **FURUTANI** does disclose a bidirectional input/output circuit in col. 13, lines 23 - 38, which states:

> Further, in the construction shown in FIG. 1, input/output circuit 6 is shown to receive and supply external write data Din and external read data Dout through different terminals. **The terminal for receiving an external write data and the terminal for outputting an external read data may share a common terminal.** In such a common pin configuration input/output circuit 6 further receives an internal control signal /ODE for controlling the output operation. The output enable control signal /ODE is generated by control signal generating circuit 405 in response to an externally applied output enable signal /OE. **Although this construction may be employed, it is assumed that inputting and outputting of the data are performed through different pin terminals in the following description**. [emphasis added by Applicants]

However, even in connection with the bidirectional circuit of col. 13 of **FURUTANI**, there is no recognition of the problem of wasted current consumption in such a bidirectional circuit. Rather, the circuit described in col. 13, lines 26 - 29 of **FURUTANI** is like that described in connection with the prior art, **with no teaching or suggestion of deactivating (turning off) the input circuit based on an activation signal**, as required by Applicants' claims 1 - 7. Rather, as shown in

Fig. 3 of **FURUTANI**, the input circuit portion of the input/output circuit 6 of **FURUTANI** includes the inverters 43, 44 and 45. The inverters 43 and 44 of **FURUTANI** each have a control input by means of which the inverting function of the inverters 43 and 44 can be set. Col. 12 of **FURUTANI**, lines 61 - 68, quoted above, indicate that the input circuit of **FURUTANI** "responds to a write instructing signal /WDE to produce an internal write data from an external write data Din". Applicants believe that this portion of **FURUTANI** indicates that under control of the write instructing signal /WDE, the external write data Din is applied to the lines IO and /IO. Applicants' believe that there **is no teaching or suggestion** in **FURUTANI** that the inverters 43 and 44 **are switched off**, based on the signal /WDE to avoid **any** power consumption, as is required by Applicants' claims 1 - 7. Rather, in **FURUTANI**, the function of the inverters 43 and 44 are merely adapted to **depend on the control signal**.

As such, Applicants' believe that **FURUTANI** fails to teach or suggest, among other limitations, in a bidirectional input/output circuit, the input circuit being deactivated based on said activation signal **such that the deactivated input circuit does not draw any quiescent or switching current as a result of the detection of received signals**, as required

by Applicants' claims 1 - 7. As such, Applicants' believe that claims 1 - 7 are patentable over the **FURUTANI** reference.

Additionally, Applicants have provided new claims 8 - 10, which are additionally believed patentable. New independent claims 8 and 11 include the control circuit of former claim 5, but additionally further describes that control circuit. The claims are supported by page 11 of the instant application, lines 4 - 15, as well as Fig. 3 of the instant application.

Although **FURUTANI** discloses in col. 13, lines 1 - 16 a **control signal generating circuit 405** which generates various internal control signals in response to externally applied control signals, i.e., a row address strobe signal /RAS, a column address strobe signal /CAS and a write enable signal /WE, **FURUTANI** fails to describe or suggest any specific implementation of that circuit. Even the ϕA generating portion of control signal generating circuit 405 of **FURUTANI**, shown in Fig. 5A of **FURUTANI** is shown only in general. As such, it is believed that **FURUTANI** fails to teach or suggest the particular combination of elements making up Applicants' new independent claims 8 and 11.

New claims 9 and 10 depend from independent claims 8 and 5, respectively, and are additionally believed to be allowable

over **FURUTANI**. New claims 9 and 10 recite, among other limitations, that the control circuit activates or deactivates said activation signal following a time delay after a change in signal level of at least one of the following signals, a circuit select signal, a word line activation signal, a bit line activation signal, and a write signal. These claims are supported in the instant specification on page 12, lines 16 - 24, and further, by Fig. 4 of the instant application.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1, 5, 7, 8 and 11. Claims 1, 5, 7, 8 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1, 5 or 8.

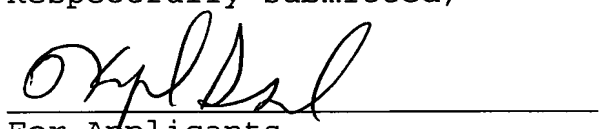
In view of the foregoing, reconsideration and allowance of claims 1 - 2 and 4 - 11 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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